7.6 A 16.7M Color VGA Display Driver IC with Partial Graphic RAM and 500Mb/s/ch Serial Interface for Mobile a-Si TFT-LCDs

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To meet the incessant demand for more functionality, smaller form factor, lower power consumption, and lower cost, a one-chip VGA display driver IC (DDI) featuring partial graphic random-access memory (GRAM) and a high-speed serial interface (HSSI) has been developed. It pairs with a 1.98 inch VGA amorphous-silicon (a-Si) TFT-LCD panel with a pixel density of 400ppi to form one of the most advanced display solutions for mobile applications. The prior state of the art for a one-chip a-Si TFT-LCD DDI was limited to QVGA resolution, whereas for low-temperature polycrystalline (LTPS) technology, a system-on-panel (SOP) solution with VGA resolution has been reported [1]. Although the latter, while achieving the same resolution as the IC described here, has three relative draw-backs: first, its low panel yield still largely offsets any cost reduction gained by integrating many functions in the DDI, which translates to higher cost; second, due to the low mobility of the panel transistors, high-speed circuits such as the HSSI, which is needed for small form factor, cannot be readily integrated; and third, the large minimum feature size renders integrating useful amounts of memory impractical.

Since VGA resolution requires 480×640 pixels, the DDI integrates 1440 data drivers – to drive 480 pixels in a given row with each pixel consisting of three (RGB) sub-pixels – and a gate controller with high-voltage level shifters driving 640 gate drivers built into the a-Si TFT LCD panel (Fig. 7.6.1). The DDI also includes a gamma corrector with four preset-curve settings, a gray-scale amplifier supporting 16.7M color depth, a built-in power-supply circuit utilizing DC-DC converters, a 115kb partial GRAM, a 624kHz internal oscillator, 24 bits of write-once non-volatile memory for house-keeping purposes and three types of I/O interfaces (I/Fs): a 16/18/24-line parallel RGB I/F, a 3-wire 9b serial I/F and a 500Mb/s/ch HSSI. To enable a trade-off between flicker reduction and power consumption, the driving mode can be set to either a dot- or line-inversion type.

Figure 7.6.2 shows a block diagram of the data driver. It includes a simplified version of the 3-level 5-phase charge recycler described in [2] for power conservation. Multiplexers and polarity controllers have been utilized to implement the charge recycling operation, in addition to the dot- and line-inversion driving operations. To implement just the line-inversion driving, alternately incorporating positive and negative polarity buffers into the data drivers would have been sufficient, but polarity inverters have also been added to enable the dot-inversion driving. Since the data driver layout size significantly affects the overall IC die size, a large portion of the development effort was directed toward its minimization. Consequently, the strategy followed for compact layout was to pair every two adjacent data buffers in the arrangement shown in Fig. 7.6.3 because it was difficult to minimize the width of the gamma decoder to match that of the buffer without unduly increasing its height. The resulting area of a data driver pair, including two gamma decoders, is 30μm×450μm. The gamma decoders along with a gray-scale amplifier and a gamma corrector constitute functionally what is generally referred to as the resistor-string DAC (R-DAC). This partitioning was driven by the need for efficient layout. The gray-scale amplifier outputs 256 reference voltages from which one voltage is selected by a decoder and passed on to a data buffer. Three such voltages comprising RGB sub-pixels determine the color of a pixel, which translates to a color depth of 16.7M. Furthermore, the resulting effective gamma (or transmission) curve, which satisfies the $f(x) = x^{\gamma}$ relationship, can be adjusted in one of 896 different ways via the gamma corrector. At power up, the gamma curve is initialized to one of the 4 preset values corresponding to γ = 1, 1.8, 2.2 or 2.5. The maximum output voltage deviation (ΔV_o) measurements of data drivers over the full gray-scale have been plotted in Fig. 7.6.4. A total of 27mW is dissipated by the data drivers and the gamma blocks.

Recent advances in a-Si TFT technology allow the integration of simple circuits like gate drivers into LCD panels, substantially reducing the circuitry associated with gate driving in a DDI; a total of 640 gate drivers have been integrated into the panel that pairs with the IC described here. The gate controller in the IC generates timing control signals synchronized to the in-coming data stream and shifts them to higher voltage levels, with typical low-to-high voltage swings of 27V, for the gate drivers in the panel.

When two nominal power supply voltages of 1.8V and 2.75V are externally provided to the built-in power-supply circuit, its internal DC-DC converters generate the 9 supply voltages necessary for driving an LCD panel. Of the 9, 2 positive and negative voltages for the gate controller are generated by boosting the internal reference voltage by 2.5 to 7 times; these voltages range from 7.75 to 19.25V and -4.65 to -16.5V, respectively. For the data drivers and the gamma blocks, the voltages vary in the ±(3 to 5.5V) ranges, corresponding to boosting factors of 1.5 to 2.75 times. Their exact voltage levels are determined by internal register values. A power-up sequence lasting 100ms is observed to avoid latch-up.

The serial I/F is used for sending control commands and updating the partial GRAM, which is used to display small sub-regions of the main display. The main display can be updated through two types of I/Fs, a parallel RGB I/F and a HSSI. Pixel information can be sent via 28 parallel lines (24 lines for RGB, 4 lines for clock and frame synchronization) for the RGB I/F, or serially through 6 lines (2 lines for one differential clock channel and 4 lines for 2 differential data channels) for the HSSI. The HSSI shown in Fig. 7.6.5 is an improved version of the one described in [3], where the maximum data transfer rate has been increased to 500Mb/s/ch; for the two data-channel configuration, 12mW is consumed. The clock signal, which is either 1/15th or 1/30th the frequency of the data transfer rate, depending on the channel configuration, is fed into a DLL to recover the clock signal used in the original data serialization. The data signals are fed into a custom designed pre-deserializer (3b packer) to reduce the rate of the data stream by a factor of 3 to reduce the speed required of the deserializer.

The IC has been fabricated in a 0.18μm triple-well CMOS process with high-voltage transistors and has an area of 23,000μm×2,500μm (Fig. 7.6.6). A total of 1,819 pads are employed with minimum pad dimensions of 20μm×100μm for the output and 35μm×115μm for the input; the pad pitches are 15μm and 55μm, respectively. To avoid being pad-limited, the data driver pads have been laid in a staggered triple-line pattern (Fig. 7.6.3). The IC with the HSSI activated consumes 45mW. Finally, key performance parameters of the IC are summarized in Fig. 7.6.7.

References:

[1] J.-S. Yu et.al., "The Development of a 2.6 inch VGA System on Panel," *SID Int'l Symposium Dig. Tech. Papers*, vol. 37, pp. 224-226, June, 2006.
[2] Jong-Seok Kim, Deog-Kyoon Jeong and Gyudong Kim, "A Multi-Level Multi-Phase Charge-Recycling Method for Low-Power AMLCD Column Drivers," *IEEE J. Solid-State Circuits*, vol. 35, no. 1, pp. 74-84, Jan., 2000.
[3] J.-Y. Lee et.al., "A 400Mbps/ch SiDP Receiver for Mobile TFT-LCD Driver IC," *SID Int'l Symposium Dig. Tech. Papers*, vol. 37, pp. 1499-1501, June, 2006.

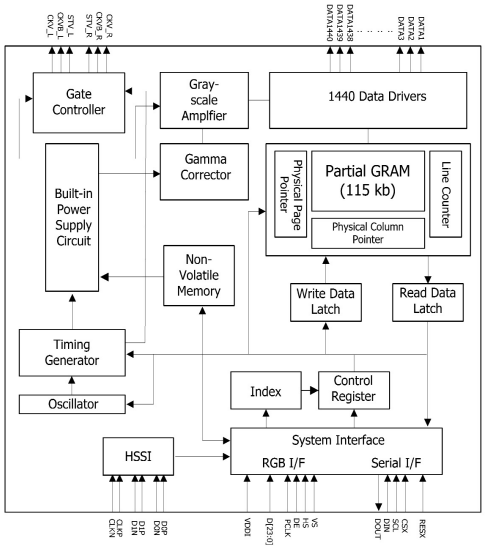

Figure 7.6.1: Block diagram of the one-chip VGA DDI.

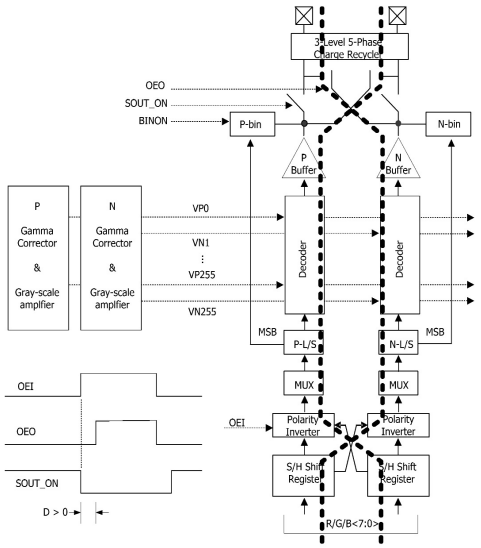

Figure 7.6.2: Block diagram of the data driver pair.

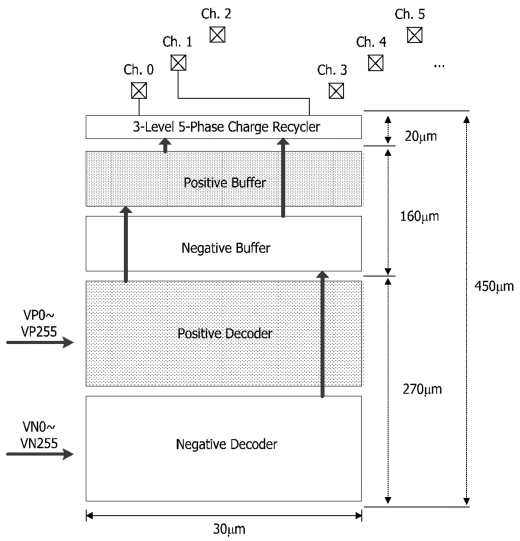

Figure 7.6.3: Floor-plan of the data driver layout with staggered pads.

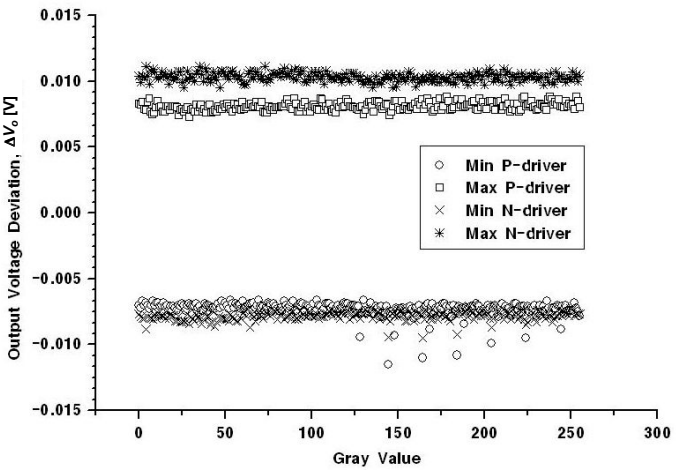

Figure 7.6.4 Measurements of maximum ΔV_0 of data drivers over the full gray-scale range.

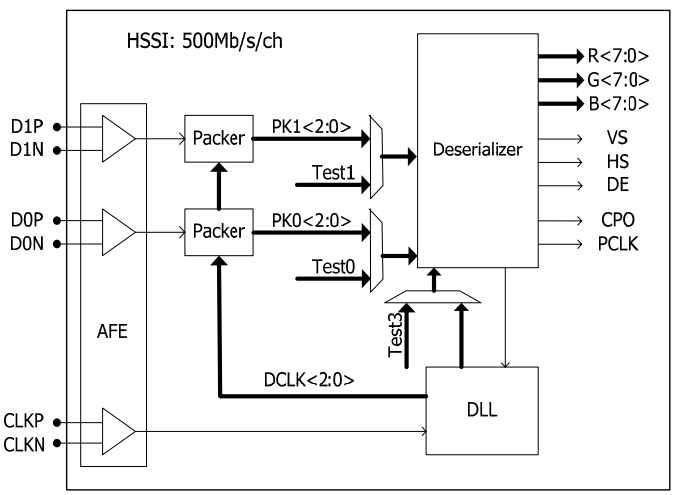

Figure 7.6.5 Block diagram of the HSSI.

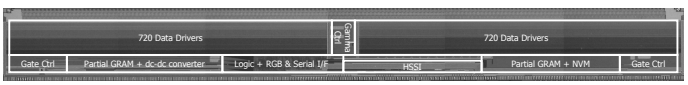

Figure 7.6.6 Micrograph of the IC (23,000μm×2,500μm).

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Technology	0.18μm triple-well CMOS
Chip size	23,000μm × 2,500μm
Partial memory size	480H × 80V × 3b = 115.2kb
Inversion methods	Dot / line (column)
Supply voltage	1.8V, 2.75V
DC-DC converter voltage	Data drive: ±3.1V~ ± 5.5V Common electrode: -1.55V~2.75V Gate driver: 7.75V~19.25V(on) / -16.5V~-4.65V(off)
Power consumption (with HSSI)	45mW
Data driver ΔV_o	< 15mV
Data driver output delay	< 5μS
Max. data transfer rate of HSSI	500Mb/s/ch.

Figure 7.6.7 Performance summary.

